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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/712,396	11/14/2003	Steven Y. Zhou	8971.0005	6846
22852	7590	12/11/2007	EXAMINER	
FINNEGAN, HENDERSON, FARABOW, GARRETT & DUNNER LLP 901 NEW YORK AVENUE, NW WASHINGTON, DC 20001-4413			DAFTUAR, SAKET K	
			ART UNIT	PAPER NUMBER
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.:	Applicant(s)	
	10/712,396	ZHOU, STEVEN Y.	
	Examiner	Art Unit	
	Saket K. Daftuar	2151	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on 14 November 2003.
- 2a) This action is FINAL. 2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 1-45 is/are pending in the application.
 - 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) Claim(s) _____ is/are allowed.
- 6) Claim(s) 1-45 is/are rejected.
- 7) Claim(s) _____ is/are objected to.
- 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 - a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____. |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____. | 6) <input type="checkbox"/> Other: _____. |

DETAILED ACTION

1. Claims 1-45 are presented for the examination.

Claim Rejections - 35 USC § 101

2. 35 U.S.C. 101 reads as follows:

Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

3. Claims 31-45 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

Claims 31-37 are directed towards a system and firewalls comprising software code that reads at the first processor. It appears that the system and firewall clusters can be implemented using "software" only and therefore, claims are directed towards non-statutory subject matter.

Claims 38-45 are directed towards a computer program product for use in a server or client mail agent. It appears that computer program product is "software" only and therefore, claims are directed towards non-statutory subject matter.

The claims lack the necessary physical articles or objects to constitute a machine or a manufacture within the meaning of 35 USC 101. They are clearly not a series of steps or acts to be a process nor are they a combination of chemical compounds to be a composition of matter. As such, they fail to fall

within a statutory category. They are, at best, functional descriptive material *per se*.

Descriptive material can be characterized as either "functional descriptive material" or "nonfunctional descriptive material." Both types of "descriptive material" are nonstatutory when claimed as descriptive material *per se*, 33 F.3d at 1360, 31 USPQ2d at 1759. When functional descriptive material is recorded on some computer-readable medium, it becomes structurally and functionally interrelated to the medium and will be statutory in most cases since use of technology permits the function of the descriptive material to be realized. Compare *In re Lowry*, 32 F.3d 1579, 1583-84, 32 USPQ2d 1031, 1035 (Fed. Cir. 1994)

Merely claiming nonfunctional descriptive material, i.e., abstract ideas, stored on a computer-readable medium, in a computer, or on an electromagnetic carrier signal, does not make it statutory. See *Diehr*, 450 U.S. at 185-86, 209 USPQ at 8 (noting that the claims for an algorithm in *Benson* were unpatentable as abstract ideas because "[t]he sole practical application of the algorithm was in connection with the programming of a general purpose computer.").

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 10-23 and 31-36 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 10 recites the limitation "first one of the processors" in "the first processor". There is insufficient antecedent basis for this limitation in the claim.

Claim 31 recites the limitation "first one of the processors" in "the first processor". There is insufficient antecedent basis for this limitation in the claim.

Claims 11-23 and 32-36 depend on claims 10 and 31, respectively. Therefore, there are insufficient antecedent basis for the same limitation in the claims.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 1-14, 17-19, 21-22, 27-28, 30-35, 38-42 and 45 are rejected under 35 U.S.C. 102(b) as being anticipated by Partridge et al US Patent Number 6,160,811 (hereinafter Partridge).

As per claim 1, Partridge discloses receiving, at a first processor, a first packet (column 2, lines 11-17); determining as a function of a multidimensional space for representing addresses [data link format for header, column 2, lines

25-26] processed by a set of data processors, a first address for the first packet (see Figure 1, column 3,line 65 – column 4,line 11); and forwarding the first packet based on the determined first address (see Figure 1, column 3,line 65 – column 4,line 11).

As per claim 2, Partridge discloses using an N-tuple space as the multidimensional space (see figures 1-2 and 4-5, data link format for header).

As per claim 3, Partridge discloses assigning to the first processor a first region based on the N-tuple space (see figures 1-2 and 4-5, data link format for header).

As per claim 4, Partridge discloses using the first address, such that the first address represents a point within the first region (see Figures 1-2 and 4-5, column 3, line 65 – column 4, line 32).

As per claim 5, Partridge discloses using N address values as the N-tuple, such that the N address values represent the point (see Figures 1-2 and 4-5, column 3, line 65 – column 4, line 32).

As per claim 6, Partridge discloses using the N-tuple space, such that N is equal to a value of at least two (see Figures 1-2 and 4-5, column 3, line 65 – column 4, line 32).

As per claim 7, Partridge discloses assigning to a second processor a second region based on the N-tuple space, such that the first region is separate from the second region (see figures 1-2 and 4-5, data link format for header).

As per claim 8, Partridge discloses forwarding, at the second processor, a second packet with a second address determined based on the second region, such that the second packet does not conflict with the first packet (see Figure 1, column 3,line 65 – column 4,line 11 and column 4, lines 22- 32).

As per claim 9, Partridge discloses forwarding, at the second processor, a second packet with a second address determined based on the second region, such that the second address does not conflict with the first address (see Figure 1, column 3,line 65 – column 4,line 11 and column 4, lines 22- 32).

As per claim 10, Partridge discloses receiving, at a first one of the processors, a packet (column 2, lines 11-17); reading, at the first processor, an N-tuple [data link format for header] address of the received packet (see Figure 1, column 3,line 65 – column 4,line 11); determining whether the N-tuple address is within an N-tuple space assigned to the first processor (see Figure 1, column 3,line 65 – column 4,line 32); sending the packet with the N-tuple address, when it is determined that the N- tuple address is within the N-tuple space assigned to the first processor (see Figure 1, column 3,line 65 – column 4, line 32) ; and determining a modified [TSU modifies the header] N-tuple address, when it is determined that the N- tuple address is not within the N-tuple space assigned to the first processor and sending the packet with the modified N-tuple address (see Figure 1, column 3,line 65 – column 4,line 32).

As per claim 11, Partridge discloses reading as the N-tuple address [reading headers of network packet address], a plurality of values from the received packet (see Figure 1, column 3, line 65 – column 4, line 32).

As per claim 12, Partridge discloses reading at least a source port (column 1, lines 18-19, column 2, and lines 11-13).

As per claim 13, Partridge discloses determining whether the N-tuple address is within the N-tuple space based on a comparison between the N-tuple address of the packet and the N-tuple space assigned to the first processor (see Figures 1-2, column 3, line 65 – column 4, line 32, column 4, line 56 – column 5, line 43).

As per claim 14, Partridge discloses determining whether the N-tuple address of the packet is within the N-tuple space based a quadrant identifier [link level id] value, wherein the quadrant identifier value corresponds to the first processor (see Figures 1-5, column 3, line 65 – column 4, line 32, column 4, line 56 – column 5, line 43).

As per claim 17, Partridge discloses adding a value to the N-tuple address, such that the modified N-tuple address is within the N-tuple space assigned to the first processor (see Figures 1-2, column 3, line 65 – column 4, line 32, column 4, line 56 – column 5, line 43).

As per claim 18, Partridge discloses modifying the N-tuple address based on the quadrant identifier value (see Figures 1-2, column 3, line 65 – column 4, line 32, column 4, line 56 – column 5, line 43).

As per claim 19, Partridge discloses sending the packet with the N-tuple address, such that the packet does not conflict with another N-tuple address associated with a second one of the processors (see Figure 1, column 3, line 65 – column 4, line 11 and column 4, lines 22- 32).

As per claim 21, Partridge discloses using a computer as the first processor (column 1, lines 8-10, column 3, and line 65).

As per claim 22, Partridge discloses using a router as the first processor (column 1, line 11, column 3, and line 65).

As per claims 27, 30, and 45, claim 27, 30 and 45 do not teach or further define over the limitation as recited in claim 1. Therefore, claims 27, 30 and 45 are rejected under same scopes as discussed in claim1, supra.

As per claim 28, claim 28 does not teach or further define over the limitation as recited in claim 10. Therefore, claims 28 rejected under same scopes as discussed in claim 10, supra.

As per claims 31-35 and 38-42, claims 31-35 and 38-42 do not teach or further define over the limitations as recited in claims 10-14. Therefore, claims 31-35 and 38-42 are rejected under same scopes as discussed in claims 10-14, supra.

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

9. Claims 15-16, 20, 23-26, 29, 36-37, and 43-44 are rejected under 35 U.S.C. 103(a) as being unpatentable over Partridge as applied to claims 1-14, 17-19, 21-22, 27-28, 30-35, 38-42 and 45 above and Le Pennec US Patent Number 7,299,353 B2 (hereinafter Le Pennec) and further in view of End III US Patent Number 7,185,041 B1 (hereinafter End).

Partridge discloses receiving, at a first processor, a first packet; determining as a function of a multidimensional space for representing addresses processed by a set of data processors, a first address for the first packet; and forwarding the first packet based on the determined first address.

Partridge is silent about determining the identifier value based on a hash function and a modulo division.

As per claims 15, 36, and 43, End teaches determining the identifier value based on a hash function (see column 4, lines 17-62).

As per claim 16, End teaches determining the identifier value based on a hash function and a modulo division (see column 4, lines 17-62).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to combine the teachings of Partridge and End to obtain the predictable result to provide an enhanced packet switched data handling system to a high speed network device securely switching data between

the high speed network devices using a enhanced hash function and arithmetic operations.

As per claim 24, Partridge discloses receiving, at a first one of the processors, a packet column 2, lines 11-17); reading, at the first processor, an N-tuple [data link format for header] address of the received packet (see Figure 1, column 3,line 65 – column 4,line 11); determining whether the read N-tuple address corresponds to the first processor based on the quadrant identifier (see Figure 1, column 3,line 65 – column 4,line 32); sending the packet with the N-tuple address, when the quadrant identifier corresponds to the first processor (see Figure 1, column 3,line 65 – column 4, line 32); and determining a modified [TSU modifies the header] N-tuple address, when the quadrant identifier does not corresponds to the first processor and sending the packet with the modified N-tuple address(see Figure 1, column 3,line 65 – column 4, line 32).

However Partridge is silent about the quadrant identifier based on a hash function, and modulo division.

End teaches the quadrant identifier based on a hash function, and modulo division (see column 4, lines 18-62).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to combine the teachings of Partridge and End to obtain the predictable result to provide a enhanced packet switched data handling system to a high speed network device securely switching data between

the high speed network devices using a enhanced hash function and arithmetic operations.

As per claim 24, Partridge discloses receiving, at a first one of the processors, a packet column 2, lines 11-17); reading, at the first processor, an N-tuple [data link format for header] address of the received packet (see Figure 1, column 3,line 65 – column 4,line 11); determining whether the read N-tuple address corresponds to the first processor based on the quadrant identifier (see Figure 1, column 3,line 65 – column 4,line 32); sending the packet with the N-tuple address, when the quadrant identifier corresponds to the first processor (see Figure 1, column 3,line 65 – column 4, line 32); and determining a modified [TSU modifies the header] N-tuple address, when the quadrant identifier does not corresponds to the first processor and sending the packet with the modified N-tuple address(see Figure 1, column 3,line 65 – column 4, line 32).

However Partridge is silent about the quadrant identifier based on a hash function, and modulo division.

End teaches the quadrant identifier based on a hash function, and modulo division (see column 4, lines 18-62).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to combine the teachings of Partridge and End to obtain the predictable result to provide a enhanced packet switched data handling system to a high speed network device securely switching data between

the high speed network devices using a enhanced hash function and arithmetic operations.

As per claim 20, 23, and 25-26 Partridge is silent about the use of firewalls as the first processor.

As per claim 20, Le Pennec teaches using a firewall as the first processor (column 3, lines 19-30).

As per claim 23, Le Pennec teaches using one or more firewalls as the set of processors, such that the one or more firewalls form a firewall cluster (column 3, lines 19-30).

As per claim 25, Le Pennec teaches assigning each of the set of processors a firewall node number (column 3, lines 19-30).

As per claim 26, Le Pennec teaches determining whether the N-tuple address corresponds to the first processor based on firewall node number (column 3, lines 19-30).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to combine the teachings of Partridge, Le Pennec and End to obtain the predictable result to provide a enhanced packet switched and data filtering and protecting system to a high speed network device being secure from firewall to switch data securely between the high speed network devices using a enhanced hash function and arithmetic operations.

As per claims 29, 37, and 44, claim 29, 37 and 44 do not teach or further define over the limitation as recited in claim 24. Therefore, claims 29, 37 and 44 are rejected under same scopes as discussed in claim 24, supra.

Conclusion

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Also, see accompanying PTO 892 form.
 - a. System and method for detecting and countering a network attack by Etheridge et al. US Publication Number 2004/0054925 A1.
 - b. Hash-based systems and methods for detecting, preventing, and tracing network worms and viruses by Milliken US Publication Number 2003/0115485 A1.
 - c. Dynamic packet filter utilizing session tracking by Goldberg et al. US Publication Number 2004/0013112 A1.
 - d. IP datagram over multiple queue pairs by Graham et al. US Patent Number 7,133,405 B2.
 - e. Handling packet fragments in a distributed network service environment by Albert et al. US Patent Number 6,742,045 B1.
11. A shortened statutory period for reply to this non-final action is set to expire **THREE MONTHS** from the mailing date of this action. Failure to respond within the period for response will result in **ABANDONMENT** of the applicant (See 35 U.S.C 133, M.P.E.P 710.02,71002 (b)).

Contact Information

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Saket K. Daftuar whose telephone number is 571-272-8363. The examiner can normally be reached on 8:30am-5:00pm M-W.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Follansbee can be reached on 571-272-3964. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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